AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Withdrawn) A semiconductor device comprising:

a base layer formed over a substrate having an insulating surface;

an insulating layer and at least one of a gate wiring and a gate electrode formed over the base layer;

a gate insulating film formed over one of the gate wiring and the gate electrode; and

an active layer of a thin film transistor including at least a channel formation region over the gate insulating film;

a source wiring and an electrode formed over the active layer; and

a pixel electrode formed over the electrode,

wherein one of the gate wiring and the gate electrode contains a resin and has the same film thickness as that of the insulating layer.

2. (Withdrawn) A semiconductor device according to claim 1, wherein the base layer comprises a material selected from the group consisting of a transition metal, an oxide of said transition metal, a nitride of said transition metal, and an oxynitride of said transition metal.

3. (Withdrawn) A semiconductor device according to claim 2, wherein the transition metal comprises a material selected from the group consisting of Sc, Ti, Cr, Ni, V, Mn, Fe, Co, Cu, Zn.

4. (Withdrawn) A semiconductor device according to claim 1, wherein the active layer of the thin film transistor is a non-single crystalline semiconductor film or a polycrystalline semiconductor film added with hydrogen or halogen hydrogen.

5. (Withdrawn) A semiconductor device according to claim 1, the width of the gate electrode of the thin film transistor is from 5 μm to 100 μm.

6. (Withdrawn) A semiconductor device according to claim 1, wherein the length of the gate electrode width of the thin film transistor is shorter than that of the thickness of the gate electrode of the thin film transistor.

7. (Withdrawn) A semiconductor device according to claim 1, wherein a surface including an upper surface of the gate wiring or the gate electrode and a surface including an upper surface of the insulating layer are in the same plane.

8. (Withdrawn) A semiconductor device according to claim 1, wherein a P–V value of a projection and a depression on an upper surface of the insulating layer is less than 20 nm.

9. (Withdrawn) A semiconductor device according to claim 1, wherein P–V value of a projection and a depression on the upper surface of the gate wiring or gate electrode is lower than 20 nm.

10. (Withdrawn) A semiconductor device according to claim 1, further comprising: a liquid crystal display device including a second substrate opposing to the substrate, and a liquid crystal interposed between a pair of substrates composed of the substrate and the second substrate.

11. (Withdrawn) A semiconductor device according to claim 1, further comprising a plurality of light emitting elements including a cathode, a layer containing an organic compound and a anode.

12. (Withdrawn) A semiconductor device according to claim 1, wherein the semiconductor device is an interactive video/ audio communication device or a general-purpose remote control device.

13. (Withdrawn) A semiconductor device comprising:

an insulating layer and at least one of a gate wiring and a gate electrode formed over a substrate having an insulating surface;

a gate insulating film formed over one of the gate wiring and the gate electrode; and

an active layer of a thin film transistor including at least a channel formation region over the gate insulating film;

a source wiring and an electrode formed over the active layer; and

a pixel electrode formed over the electrode,

wherein one of the gate wiring and the gate electrode contains a resin and has the same film thickness as that of the insulating layer.

14. (Withdrawn) A semiconductor device according to claim 13, wherein the length of the gate electrode width of the thin film transistor is shorter than that of the thickness of the gate electrode of the thin film transistor.

15. (Withdrawn) A semiconductor device according to claim 13, wherein a surface including an upper surface of the gate wiring or the gate electrode and a surface including an upper surface of the insulating layer are in the same plane.

16. (Withdrawn) A semiconductor device according to claim 13, further comprising: a liquid crystal display device including a second substrate opposing to the substrate, and a liquid crystal interposed between a pair of substrates composed of the substrate and the second substrate.

17. (Withdrawn) A semiconductor device according to claim 13, further comprising a plurality of light emitting elements including a cathode, a layer containing an organic compound and a anode.

18. (Withdrawn) A semiconductor device according to claim 13, wherein the semiconductor device is an interactive video/ audio communication device or a general-purpose remote control device.

19. (Original) A method for manufacturing a semiconductor device comprising the steps of:

forming a base film or performing a base pretreatment over a substrate having an insulating surface;

forming an insulating film over the substrate;

forming a mask over the insulating film;

forming a depression by selectively etching the insulating film;

forming an embedded wiring in the depression by a droplet discharge method;

removing the mask;

performing a planarization processing to an upper surface of the embedded wiring;

forming a gate insulating film over the embedded wiring; and

forming a semiconductor film over the gate insulating film.

20. (Original) A method for manufacturing a semiconductor device according to claim 19, wherein the base layer is used as an etching stopper in the step of forming the depression by selectively etching the insulating film.

21. (Original) A method for manufacturing a semiconductor device according to claim 19, wherein the planarizing process is a press treatment, a heat press treatment or a CMP processing pressing the insulating film and the embedded wiring by a press unit.

22. (Original) A method for manufacturing a semiconductor device according to claim 19, wherein the planarization processing is a heat press treatment capable of heating and pressing at the same time to perform baking of the embedded wiring.

23. (Original) A method for manufacturing a semiconductor device according to claim 19, wherein the embedded wiring is at least one of a gate electrode and gate wiring of a thin film transistor.

24. (Original) A method for manufacturing a semiconductor device according to claim 19, wherein the step of forming a mask over the insulating film comprises a step of forming a first material layer and a second material layer surrounding the first material layer,

wherein the first material layer is soluble in a first solvent, and

wherein the second material layer is soluble in a second solvent, and

wherein the first material layer and the second material layer are formed with a device comprising a plurality of nozzles capable of discharging different materials: and

a step of forming a mask comprising the first material film by removing the second material alone by the second solvent.

25. (Original) A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film over a substrate having an insulating surface;

forming a mask over the insulating film;

forming a depression by selectively etching the insulating film;

forming an embedded wiring in the depression by a droplet discharge method;

removing the mask;

performing a planarization processing to an upper surface of the embedded wiring;

forming a gate insulating film over the embedded wiring; and

forming a semiconductor film over the gate insulating film.

26. (Original) A method for manufacturing a semiconductor device according to claim 25, wherein the planarizing process is a press treatment, a heat press treatment or a CMP processing pressing the insulating film and the embedded wiring by a press unit.

27. (Original) A method for manufacturing a semiconductor device according to claim 25, wherein the planarization processing is a heat press treatment capable of heating and pressing at the same time to perform baking of the embedded wiring.

28. (Original) A method for manufacturing a semiconductor device according to claim 25, wherein the embedded wiring is at least one of a gate electrode and gate wiring of a thin film transistor.

29. (Original) A method for manufacturing a semiconductor device according to claim 25, wherein the step of forming a mask over the insulating film comprises a step of forming a first material layer and a second material layer surrounding the first material layer,

wherein the first material layer is soluble in a first solvent, and

wherein the second material layer is soluble in a second solvent, and

wherein the first material layer and the second material layer are formed with a device comprising a plurality of nozzles capable of discharging different materials: and

a step of forming a mask comprising the first material film by removing the second material alone by the second solvent.